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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,301	10/07/2005	Torayuki Tsukada	10921.359USWO	8326

52835 7590 04/10/2007
HAMRE, SCHUMANN, MUELLER & LARSON, P.C.
P.O. BOX 2902
MINNEAPOLIS, MN 55402-0902

EXAMINER

BAISA, JOSELITO SASIS

ART UNIT	PAPER NUMBER
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2832

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No. 10/552,301	Applicant(s) TSUKADA, TORAYUKI	
	Examiner Joselito Baisa	Art Unit 2832	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 October 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>10/7/2005</u> . | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Toshihiro [JP 08064401].

Toshihiro discloses resistor element 4 including an electrode-forming a surface 1; at least two electrodes (2, 3, 6 on both ends) provided at the electrode forming surface 1; and an insulating layer 8 provided at the electrode-forming surface 1; wherein the electrode-forming surface 1 includes an inter-electrode region positioned between the two electrodes (2, 3, 6 on both ends) and covered by the insulating layer 8, and wherein the insulating layer 8 has a thickness which is equal or generally equal to a thickness of the electrodes [Abstract, Figure 1; Paragraph 14].

With respect to claims 5 and 7-9, the claims are method counterpart of structure of claim 1 and method steps therefore are inherent for manufacturing a chip resistor.

Regarding claim 2, Toshihiro discloses the thickness of the insulating layer 8 is smaller than the thickness of the electrodes, and wherein difference between the thickness of the insulating layer 8 and the thickness of the electrodes is so set that, when the resistor element flexes upon receiving a load, the insulating layer comes into contact with a flat mount surface before the resistor element is damaged [Page 4, Paragraph 15].

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Regarding claim 3, Toshihiro discloses the thickness of the insulating layer is smaller than the thickness of the electrodes, and wherein difference between the thickness of the insulating layer and the thickness of the electrodes is set to be smaller than maximum deflection of the resistor element when maximum bending stress produced in the resistor element reaches elastic limit of the resistor element [Page 4, Paragraph 15].

Regarding claim 4, The chip resistor according to claim 1, wherein the insulating layer 8 is formed by thick film printing [Abstract, Paragraph 14].

With respect to claim 6, the claim is a method counterpart of structure of claim 4 and method steps therefore are inherent for manufacturing a chip resistor with an insulating layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joselito Baisa whose telephone number is (571) 272-7132. The examiner can normally be reached on M-F 5:30 am to 2:00 pm.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Elvin Enad can be reached on (571) 272-1990. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Joselito Baisa
Examiner
Art Unit 2832

jsb


ELVIN ENAD
SUPERVISORY PATENT EXAMINER
02 APRIL 07